NEC
ELECTRON DEVICE

MOS INTEGRATED CIRCUIT

μPD424100-L

4M BIT DYNAMIC CMOS RAM (FAST PAGE MODE)

DESCRIPTION

The NEC μPD424100-L is a 4194304-word by 1 bit dynamic CMOS RAM with optional fast page mode. CMOS sense amplifier, peripheral circuits and 1 transistor memory cell technique realize high speed access, cycle time and low power dissipation.

Refresh is accomplished by performing $\overline{RAS}$ only refresh cycles, hidden refresh cycles, $\overline{CAS}$ before $\overline{RAS}$ refresh cycles, or normal read or write cycles on the 1024 address combinations of A_0 to A_9, during a 128 ms period.

The μPD424100-L is packaged in 26-pin plastic SOJ, 20-pin plastic ZIP and 26-pin plastic TSOP. ★

FEATURES

- 4194304 words by 1 bit organization

DEVICE	ACCESS TIME (MAX.)	R/W CYCLE (MIN.)	PAGE MODE CYCLE (MIN.)
μPD424100-60L	60 ns	120 ns	40 ns
μPD424100-70L	70 ns	140 ns	45 ns
μPD424100-80L	80 ns	160 ns	50 ns
μPD424100-10L	100 ns	190 ns	60 ns

★

- Low power dissipation
  - Active ..... 660 mW MAX. (μPD424100-60L)
    550 mW MAX. (μPD424100-70L)
    495 mW MAX. (μPD424100-80L)
    440 mW MAX. (μPD424100-10L)
  - Standby ..... 1.1 mW MAX. (CMOS level)

★

- Single + 5 V ±10 % power supply
- On-chip substrate bias generator
- Multiplexed address inputs
- Non latched I/O, TTL-compatible
- Read-modify-write, Fast Page Mode capability
- 1024 refresh cycles /128 ms
- $\overline{RAS}$ only refresh, hidden refresh and $\overline{CAS}$ before $\overline{RAS}$ internal address refresh
- 512K words by 8 bits Test Mode capability

Document No. IC-2601B
(O.D. No. IC-8085B)
Date Published July 1992P
Printed in Japan

The mark ★ shows revised points.

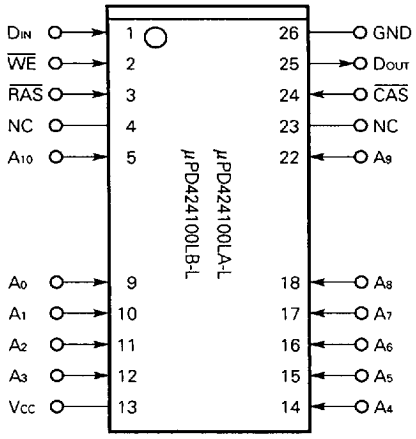
ORDERING INFORMATION ★

PART NUMBER	PACKAGE	ACCESS TIME (MAX.)	QUALITY GRADE
μPD424100LA-60L	26-pin Plastic SOJ	60 ns	STANDARD
μPD424100LA-70L	26-pin Plastic SOJ	70 ns	STANDARD
μPD424100LA-80L	26-pin Plastic SOJ	80 ns	STANDARD
μPD424100LA-10L	26-pin Plastic SOJ	100 ns	STANDARD
μPD424100LB-60L	26-pin Plastic SOJ	60 ns	STANDARD
μPD424100LB-70L	26-pin Plastic SOJ	70 ns	STANDARD
μPD424100LB-80L	26-pin Plastic SOJ	80 ns	STANDARD
μPD424100LB-10L	26-pin Plastic SOJ	100 ns	STANDARD
μPD424100V-60L	20-pin Plastic ZIP	60 ns	STANDARD
μPD424100V-70L	20-pin Plastic ZIP	70 ns	STANDARD
μPD424100V-80L	20-pin Plastic ZIP	80 ns	STANDARD
μPD424100V-10L	20-pin Plastic ZIP	100 ns	STANDARD
μPD424100GS-60L-9JD	26-pin Plastic TSOP	60 ns	STANDARD
μPD424100GS-70L-9JD	26-pin Plastic TSOP	70 ns	STANDARD
μPD424100GS-80L-9JD	26-pin Plastic TSOP	80 ns	STANDARD
μPD424100GS-10L-9JD	26-pin Plastic TSOP	100 ns	STANDARD
μPD424100GS-60L-9KD	26-pin Plastic TSOP (Reverse bent)	60 ns	STANDARD
μPD424100GS-70L-9KD	26-pin Plastic TSOP (Reverse bent)	70 ns	STANDARD
μPD424100GS-80L-9KD	26-pin Plastic TSOP (Reverse bent)	80 ns	STANDARD
μPD424100GS-10L-9KD	26-pin Plastic TSOP (Reverse bent)	100 ns	STANDARD

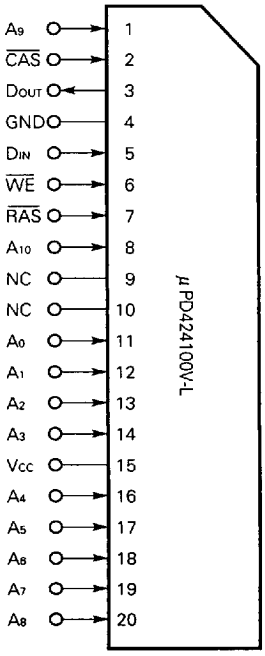
Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

PIN CONFIGURATION ★

26-pin Plastic SOJ
(Top View)

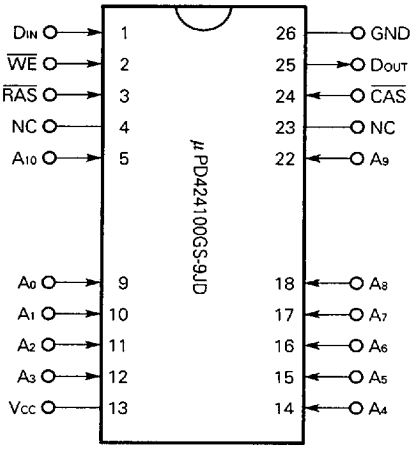


20-pin Plastic ZIP
(Front View)

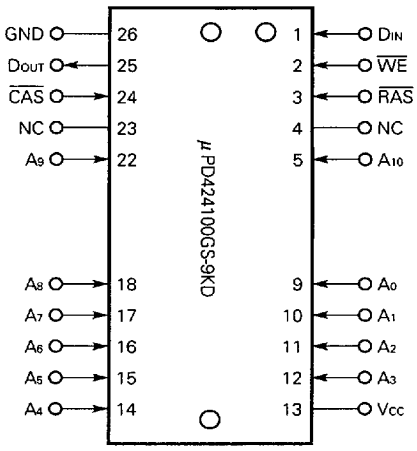


A_0 to A_{10}	:	Address Inputs
$\overline{RAS}$	:	Row Address Strobe
$\overline{CAS}$	:	Column Address Strobe
$\overline{WE}$	:	Write Enable
D_{IN}	:	Data Inputs
D_{OUT}	:	Data Outputs
V_{CC}	:	Power Supply
GND	:	Ground
NC	:	No Connection

26-pin Plastic TSOP
(Top View)



26-pin Plastic TSOP (Reverse bent)
(Top View)



ABSOLUTE MAXIMUM RATINGS*

Voltage on Any Pin Relative to GND	−1.0 to +7.0	V
Short Circuit Output Current	50	mA
Power Dissipation	1	W
Operating Temperature	0 to +70	°C
Storage Temperature	−55 to +125	°C

***COMMENT**: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational sections of this specification. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (NOTES: 1, 2)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4		V_{CC} + 1.0 V	V
Input Low Voltage	V_{IL}	−1.0		0.8	V
Ambient Temperature	T_a	0		70	°C

★ **DC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted)**

PARAMETER	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT	NOTES
Operating Current	I_{CC1}	$\overline{RAS}$, $\overline{CAS}$ Cycling $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	μPD424100-60L			120	mA	3
			μPD424100-70L			100		
			μPD424100-80L			90		
			μPD424100-10L			80		
Standby Current	I_{CC2}	$\overline{RAS} = \overline{CAS} \geq V_{IH(MIN.)}$				2	mA	
		$\overline{RAS} = \overline{CAS} \geq V_{CC} - 0.2$ V				0.2		
Refresh Current ($\overline{RAS}$ Only Refresh)	I_{CC3}	$\overline{RAS}$ Cycling, $\overline{CAS} \geq V_{IH}$, $t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	μPD424100-60L			120	mA	3
			μPD424100-70L			100		
			μPD424100-80L			90		
			μPD424100-10L			80		
Operating Current (Fast Page Mode)	I_{CC4}	$\overline{RAS} \leq V_{IL}$, $\overline{CAS}$ Cycling, $t_{PC} = t_{PC(MIN.)}$, I_O = 0 mA	μPD424100-60L			90	mA	3
			μPD424100-70L			80		
			μPD424100-80L			70		
			μPD424100-10L			60		
Refresh Current ($\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC5}	$t_{RC} = t_{RC(MIN.)}$, I_O = 0 mA	μPD424100-60L			120	mA	3
			μPD424100-70L			100		
			μPD424100-80L			90		
			μPD424100-10L			80		
Battery Back Up Current (Standby with $\overline{CAS}$ before $\overline{RAS}$ Refresh)	I_{CC6}	Stand-by: $V_{CC} - 0.2$ V $\leq \overline{RAS}$, $V_{CC} - 0.2$ V $\leq \overline{CAS}$ $\overline{CAS}$ before $\overline{RAS}$ Refresh: 1024 cycle/128 ms $\overline{RAS}$, $\overline{CAS}$: 0 V $\leq V_{IL} \leq$ 0.2 V, $V_{CC} - 0.2$ V $\leq V_{IH} \leq V_{IH}$ MAX. $\overline{WE} = V_{IH}$ Address: V_{IH} or V_{IL} Output: Hi-Z	$t_{RAS} \leq 200$ ns			300	μA	
			$t_{RAS} \leq 1$ μs			500		
Input Leakage Current	$I_{I(L)}$	V_I = 0 to 5.5 V all other pins = 0 V		−10		10	μA	
Output Leakage Current	$I_{O(L)}$	D_{OUT} is disabled V_O = 0 to 5.5 V		−10		10	μA	
Output High Voltage	V_{OH}	I_O = −5 mA		2.4			V	
Output Low Voltage	V_{OL}	I_O = 4.2 mA				0.4	V	

CAPACITANCE (T_a = 25 °C, f = 1 MHz)

PARAMETER		SYMBOL	MIN.	TYP.	MAX.	UNIT
Input Capacitance	A_0 to A_{10}, D_{IN}	C_{I1}			5	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	C_{I2}			7	pF
Output Capacitance	D_{OUT}	C_O			7	pF

AC CHARACTERISTICS (Recommended Operating Conditions unless otherwise noted) (NOTES: 2, 4, 5) ★

(1) μPD424100-60L, 424100-70L

PARAMETER	SYMBOL	μPD424100-60L		μPD424100-70L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	120		140		ns	6
Read Write Cycle Time	t_{RWC}	145		165		ns	6
Fast Page Mode Cycle Time (Read or Write)	t_{PC}	40		45		ns	6
Fast Page Mode Cycle Time (Read-modify-write)	t_{PRWC}	65		70		ns	7, 8
Access Time from $\overline{RAS}$	t_{RAC}		60		70	ns	7, 9
Access Time from $\overline{CAS}$ (Falling Edge)	t_{CAC}		15		20	ns	7, 9
Access Time from Column Address	t_{AA}		30		35	ns	7, 9
Access Time from $\overline{CAS}$ Precharge ($\overline{CAS}$ Rising Edge)	t_{ACP}		35		40	ns	7
Data Set-up Time	t_{CLZ}	0		0		ns	10
Output Buffer Turn-off Delay	t_{OFF}	0	15	0	15	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	50		60		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)	t_{RAS}	60	10000	70	10000	ns	
$\overline{RAS}$ Pulse Width (Page Mode)	t_{RASP}	60	125000	70	125000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		20		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	35		40		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	15	10000	20	10000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	60		70		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	20	40	20	50	ns	11
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		ns	12
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		ns	
$\overline{CAS}$ Precharge Time (Page Mode)	t_{CP}	10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	10		10		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	15		15		ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	15	30	15	35	ns	9
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	30		35		ns	
Read Command Set-up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	13
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	13
Write Command Hold Time	t_{WCH}	15		15		ns	
Write Command Pulse Width	t_{WP}	15		15		ns	14
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20		20		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15		15		ns	

(1) μPD424100-60L, 424100-70L

PARAMETER	SYMBOL	μPD424100-60L		μPD424100-70L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Data-in Set-up Time	t_{DS}	0		0		ns	15
Data-in Hold Time	t_{DH}	15		15		ns	15
$\overline{WE}$ Command Set-up Time	t_{WCS}	0		0		ns	16
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	20		20		ns	16
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	60		70		ns	16
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	30		35		ns	16
$\overline{CAS}$ Set-up Time for CBR Refresh	t_{CSR}	10		10		ns	
$\overline{CAS}$ Hold Time for CBR Refresh	t_{CHR}	15		15		ns	
$\overline{WE}$ Set-up Time	t_{WSR}	10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		15		ns	
Refresh Period	t_{REF}		128		128	ms	

(2) μPD424100-80L, 424100-10L

PARAMETER	SYMBOL	μPD424100-80L		μPD424100-10L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Random Read or Write Cycle Time	t_{RC}	160		190		ns	6
Read Write Cycle Time	t_{RWC}	185		220		ns	6
Fast Page Mode Cycle Time (Read or Write)	t_{PC}	50		60		ns	6
Fast Page Mode Cycle Time (Read-modify-write)	t_{PRWC}	75		90		ns	7, 8
Access Time from $\overline{RAS}$	t_{RAC}		80		100	ns	7, 9
Access Time from $\overline{CAS}$ (Falling Edge)	t_{CAC}		20		25	ns	7, 9
Access Time from Column Address	t_{AA}		40		50	ns	7, 9
Access Time from $\overline{CAS}$ Precharge ($\overline{CAS}$ Rising Edge)	t_{ACP}		45		55	ns	7
Data Set-up Time	t_{CLZ}	0		0		ns	10
Output Buffer Turn-off Delay	t_{OFF}	0	20	0	25	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	ns	
$\overline{RAS}$ Precharge Time	t_{RP}	70		80		ns	
$\overline{RAS}$ Pulse Width (Random Read, Write Cycle)	t_{RAS}	80	10000	100	10000	ns	
$\overline{RAS}$ Pulse Width (Page Mode)	t_{RASP}	80	125000	100	125000	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	20		25		ns	
$\overline{RAS}$ Hold Time from $\overline{CAS}$ Precharge	t_{RHCP}	45		55		ns	
$\overline{CAS}$ Pulse Width	t_{CAS}	20	10000	25	10000	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	80		100		ns	
$\overline{RAS}$ to $\overline{CAS}$ Delay Time	t_{RCD}	25	60	25	75	ns	11
$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	t_{CRP}	10		10		ns	12
$\overline{CAS}$ Precharge Time	t_{CPN}	10		10		ns	
$\overline{CAS}$ Precharge Time (Page Mode)	t_{CP}	10		10		ns	
$\overline{RAS}$ Precharge $\overline{CAS}$ Hold Time	t_{RPC}	10		10		ns	
Row Address Set-up Time	t_{ASR}	0		0		ns	
Row Address Hold Time	t_{RAH}	12		12		ns	
Column Address Set-up Time	t_{ASC}	0		0		ns	
Column Address Hold Time	t_{CAH}	15		20		ns	
$\overline{RAS}$ to Column Address Delay Time	t_{RAD}	17	40	17	50	ns	9
Column Address Lead Time Referenced to $\overline{RAS}$	t_{RAL}	40		50		ns	
Read Command Set-up Time	t_{RCS}	0		0		ns	
Read Command Hold Time Referenced to $\overline{RAS}$	t_{RRH}	10		10		ns	13
Read Command Hold Time Referenced to $\overline{CAS}$	t_{RCH}	0		0		ns	13
Write Command Hold Time	t_{WCH}	15		20		ns	
Write Command Pulse Width	t_{WP}	15		20		ns	14
Write Command to $\overline{RAS}$ Lead Time	t_{RWL}	20		25		ns	
Write Command to $\overline{CAS}$ Lead Time	t_{CWL}	15		20		ns	
Data-in Set-up Time	t_{DS}	0		0		ns	15
Data-in Hold Time	t_{DH}	15		20		ns	15

(2) μPD424100-80L, 424100-10L

PARAMETER	SYMBOL	μPD424100-80L		μPD424100-10L		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
$\overline{WE}$ Command Set-up Time	t_{WCS}	0		0		ns	16
$\overline{CAS}$ to $\overline{WE}$ Delay	t_{CWD}	20		25		ns	16
$\overline{RAS}$ to $\overline{WE}$ Delay	t_{RWD}	80		100		ns	16
Column Address to $\overline{WE}$ Delay Time	t_{AWD}	40		50		ns	16
$\overline{CAS}$ Set-up Time for CBR Refresh	t_{CSR}	10		10		ns	
$\overline{CAS}$ Hold Time for CBR Refresh	t_{CHR}	15		20		ns	
$\overline{WE}$ Set-up Time	t_{WSR}	10		10		ns	
$\overline{WE}$ Hold Time	t_{WHR}	15		20		ns	
Refresh Period	t_{REF}		128		128	ms	

NOTES

(1) All voltages are referenced to GND.

(2) An initial pause of 100 μs is required after power-on followed by 8 refresh ($\overline{RAS}$ only refresh or $\overline{CAS}$ before $\overline{RAS}$ refresh) cycles before proper device operation is achieved.

(3) I_{CC1}, I_{CC3}, I_{CC4} and I_{CC5} depend on output loading and cycle rates. Specified values are obtained with the output open. And further, I_{CC3} is measured on condition that column addresses in $\overline{RAS}$ only cycle are held high or low level and I_{CC4} is measured on condition that column addresses in fast page mode are changed only one time.

(4) AC measurements assume t_T = 5 ns.

(5) $V_{IH\,(MIN)}$ and $V_{IL\,(MAX)}$ are reference levels for measuring timing of input signals. Transition times are measured between V_{IH} and V_{IL}.
Access times are measured at $V_{OH\,(MIN)}$ and $V_{OL\,(MAX)}$ and loading condition is 2 TTL + 100 pF.

(6) The minimum specifications are used only to indicate cycle time at which proper operation over the full temperature range (T_a = 0 to 70 °C) is assured.

(7) Load = 2 TTL loads and 100 pF.

(8) Assumes that $t_{RCD} \leq t_{RCD\,(MAX)}$. If t_{RCD} is greater than the maximum specified value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the value shown.

(9) If t_{RAD} is greater than $t_{RAD\,(MAX.)}$, then access time is defined by t_{AA}.

(10) $t_{OFF\,(MAX)}$ defines the time at which the output achieves the open circuit condition and is not referenced to V_{OH} or V_{OL}.

(11) Operation within the $t_{RCD\,(MAX)}$ limit insures that $t_{RAC\,(MAX)}$ can be met. $t_{RCD\,(MAX)}$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD\,(MAX)}$ limit, then access time is controlled exclusively by t_{CAC}.

(12) t_{CRP} requirement should be applicable for $\overline{RAS}$/$\overline{CAS}$ cycles preceded by any cycles.

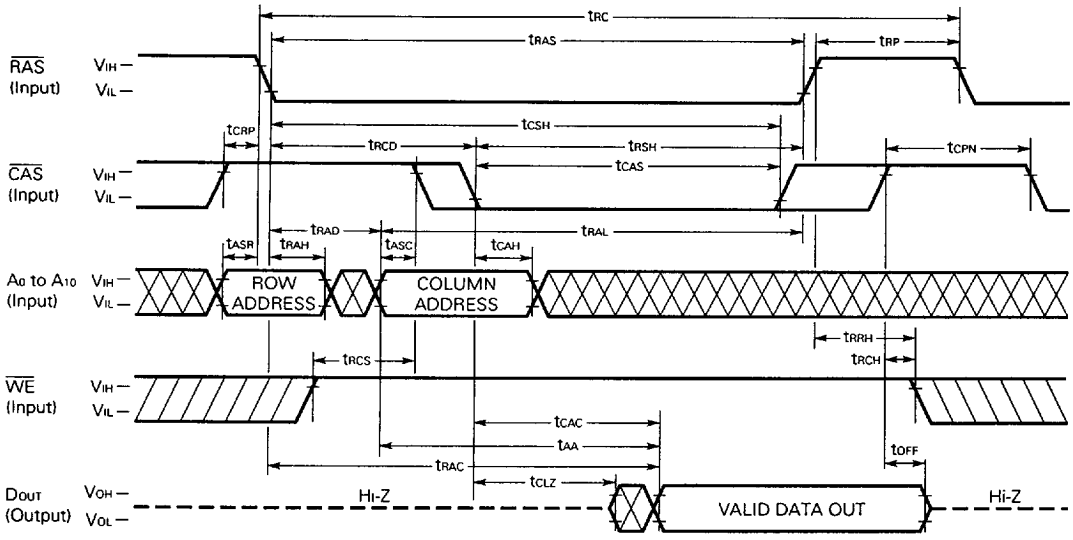
(13) Either t_{RRH} or t_{RCH} must be satisfied for a read cycle.

(14) t_{WP} is applicable for delayed write cycle. If the cycle is early write, it should be satisfied the specified value of t_{WCH}.

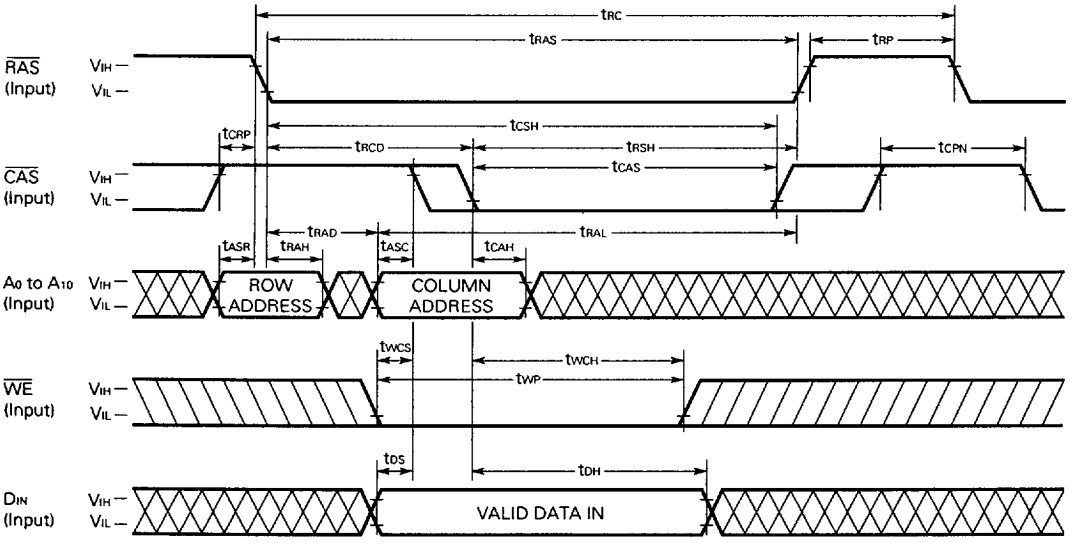
(15) These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WE}$ leading edge in delayed write or read-modify-write cycles.

(16) t_{WCS}, t_{CWD}, t_{RWD} and t_{AWD} are restrictive operating parameters in read-write and read-modify-write cycles only. If $t_{WCS} \geq t_{WCS\,(MIN)}$ the cycle is an early write cycle and the data output will remain open circuit throughout the entire cycle. If $t_{CWD} \geq t_{CWD\,(MIN)}$, $t_{RWD} \geq t_{RWD\,(MIN)}$, $t_{AWD} \geq t_{AWD\,(MIN)}$ the cycle is a read-write and the data output will contain data read from the selected cell. If neither of the above conditions are met, the condition of the data out (at access time and until $\overline{CAS}$ goes back to V_{IH}) is indeterminate.

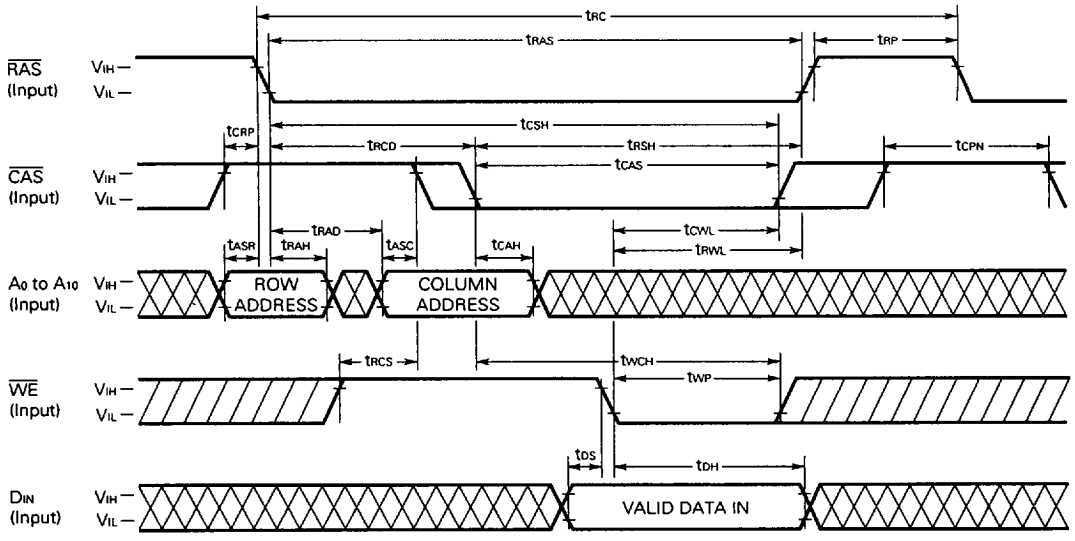
READ MODE



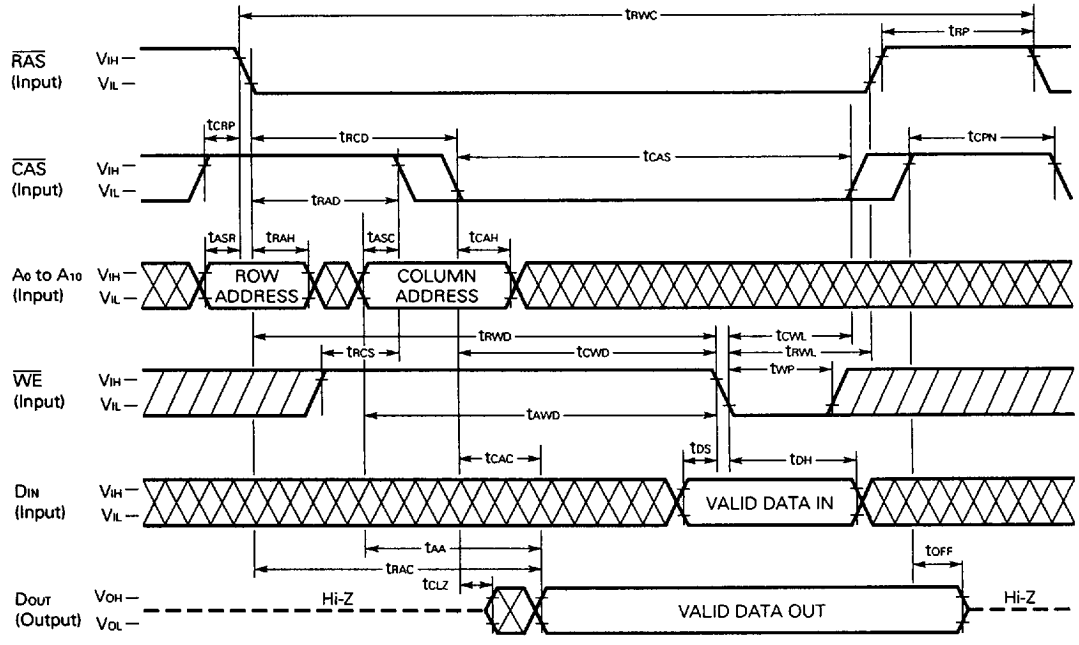
EARLY WRITE CYCLE



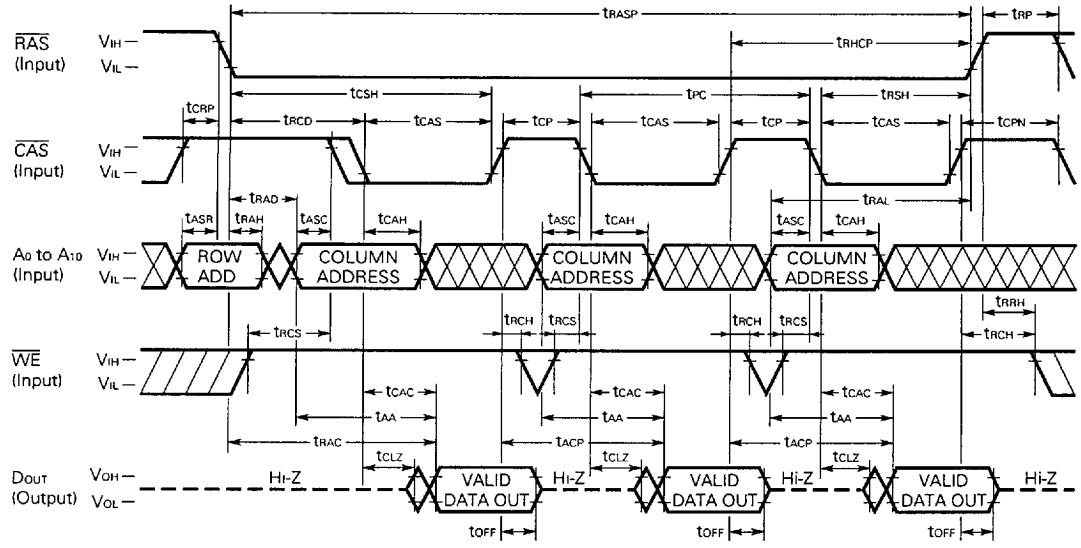
LATE WRITE CYCLE



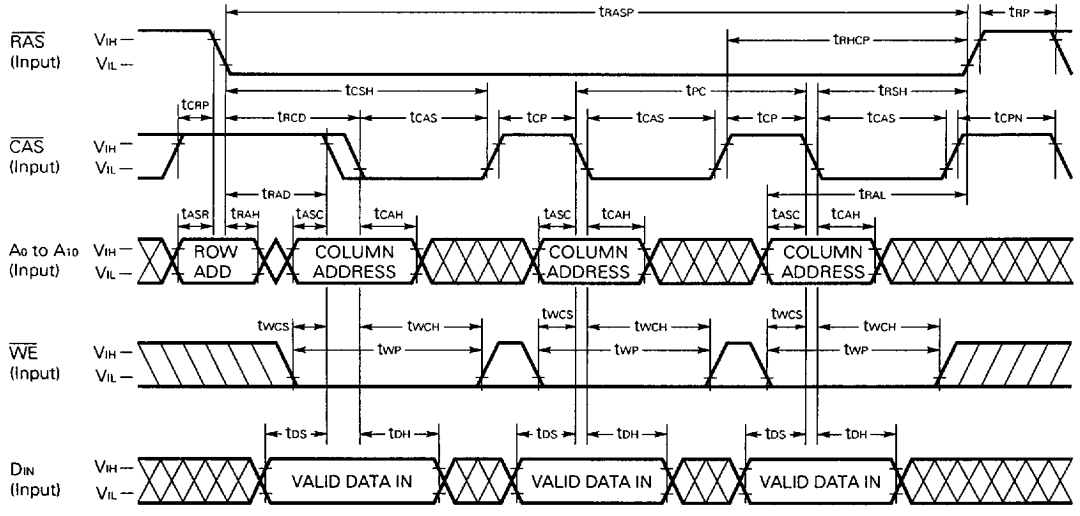
READ-WRITE/READ-MODIFY-WRITE CYCLE



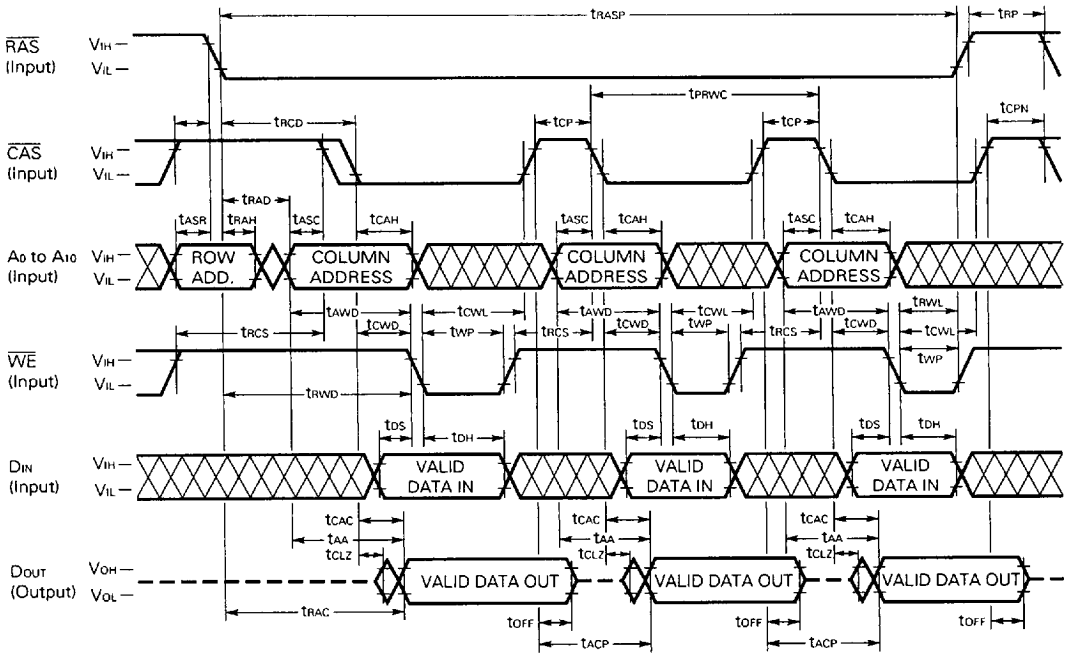
PAGE MODE READ CYCLE



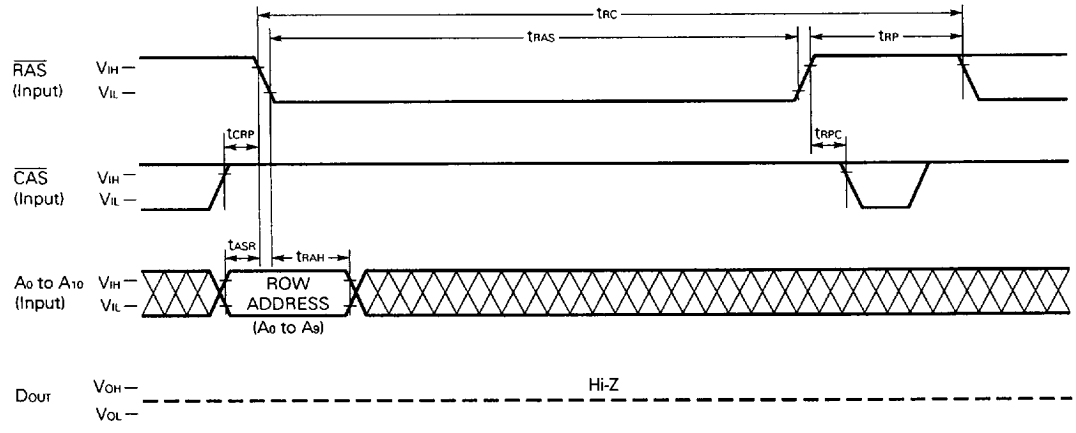
PAGE MODE EARLY WRITE CYCLE



PAGE MODE READ-WRITE/READ-MODIFY-WRITE CYCLE



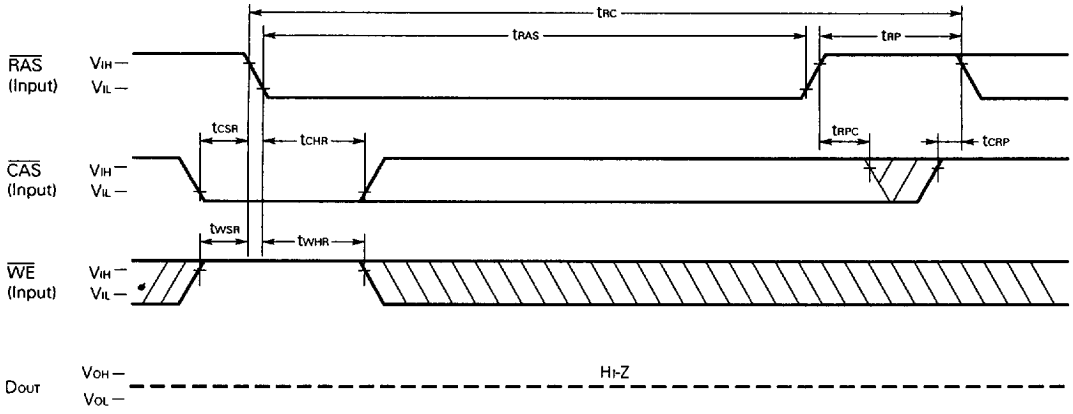
RAS ONLY REFRESH CYCLE



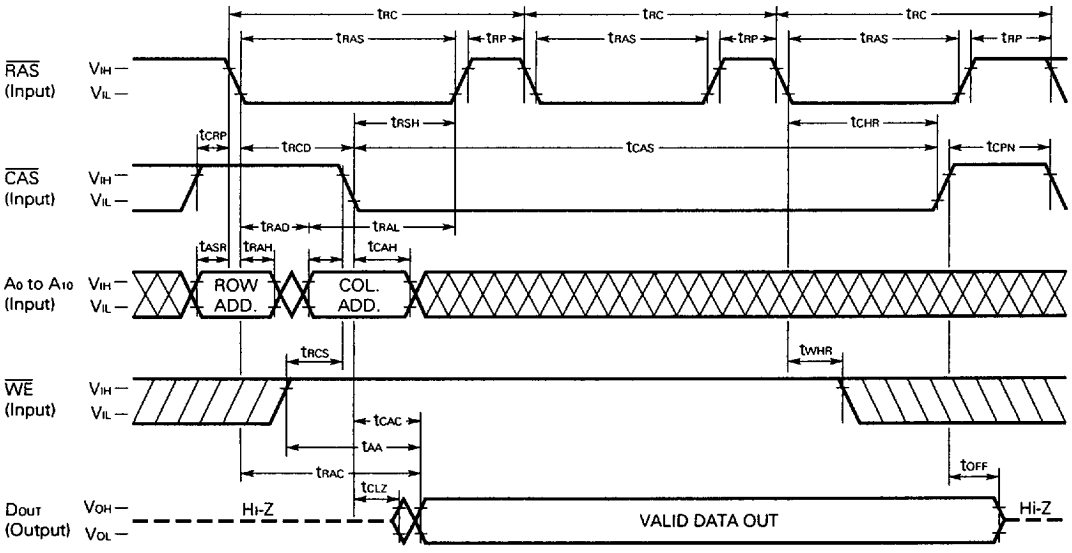
WE Don't Care

* Although A10 is not necessary for refreshing, the specifications of both tASR, tRAH are defined in RAS only refresh cycle.

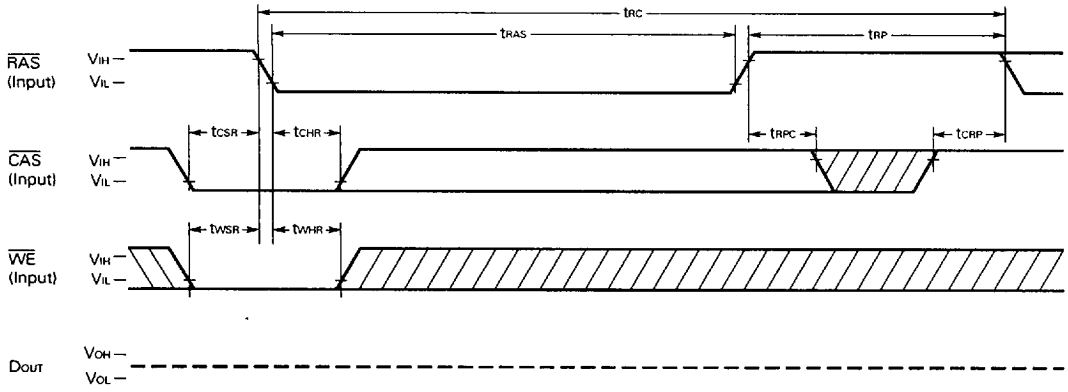
$\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE



HIDDEN REFRESH CYCLE



TEST MODE SET CYCLE ($\overline{WE}$ AND $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH CYCLE)



TEST MODE

TEST MODE is fast test function. On using this mode, test time is reduced to 1/8. In this TEST MODE, internal organization is 512K words by 8-bit apparently. The input levels of the $\overline{RAS}$ input A10 and $\overline{CAS}$ input A0, A10 are Don't care.

1. How to enter into TEST MODE
   Through TEST MODE SET CYCLE ($\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle), the device is entered into TEST MODE.

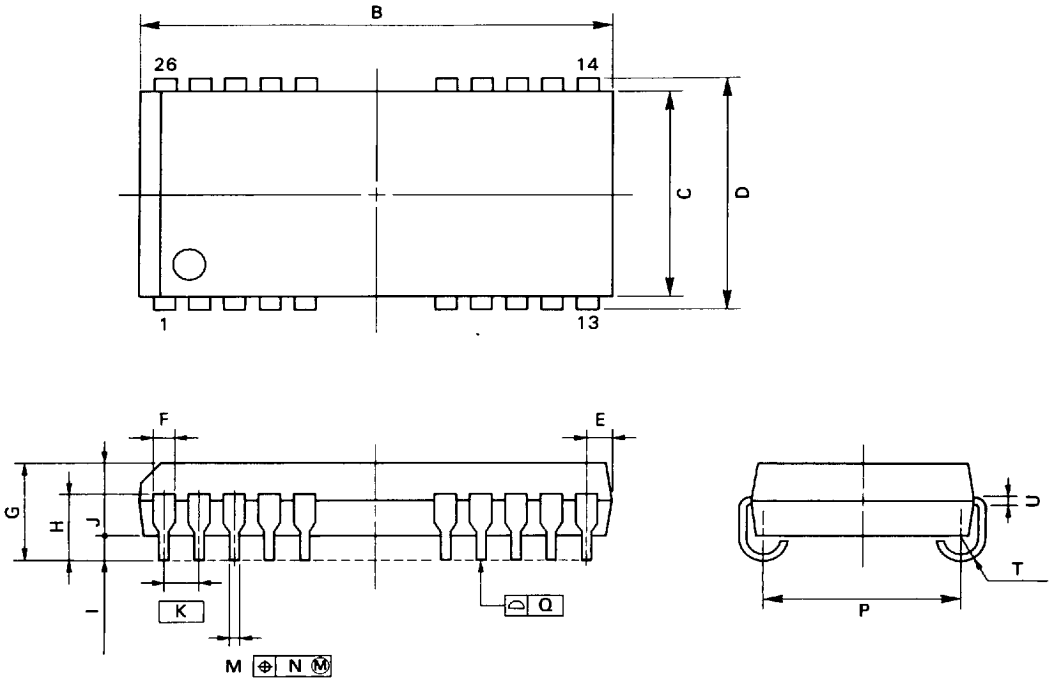
2. Write/Read in TEST MODE
   Write data of "1" or "0" through DIN by controlling address except for above-mentioned address. So equal data is written all 8 bits. And read through DOUT to check written data. In case of writing all 8 bits rightly, the data is "1". But wrong, the data is "0".

3. Refresh in TEST MODE
   Use normal read cycle or $\overline{WE}$ and $\overline{CAS}$ before $\overline{RAS}$ refresh cycle.

4. How to exit TEST MODE
   Through $\overline{RAS}$ only refresh cycle or $\overline{CAS}$ before $\overline{RAS}$ refresh cycle, the device is exitted TEST MODE.

PACKAGE INFORMATION

26PIN PLASTIC SOJ (300 mil)



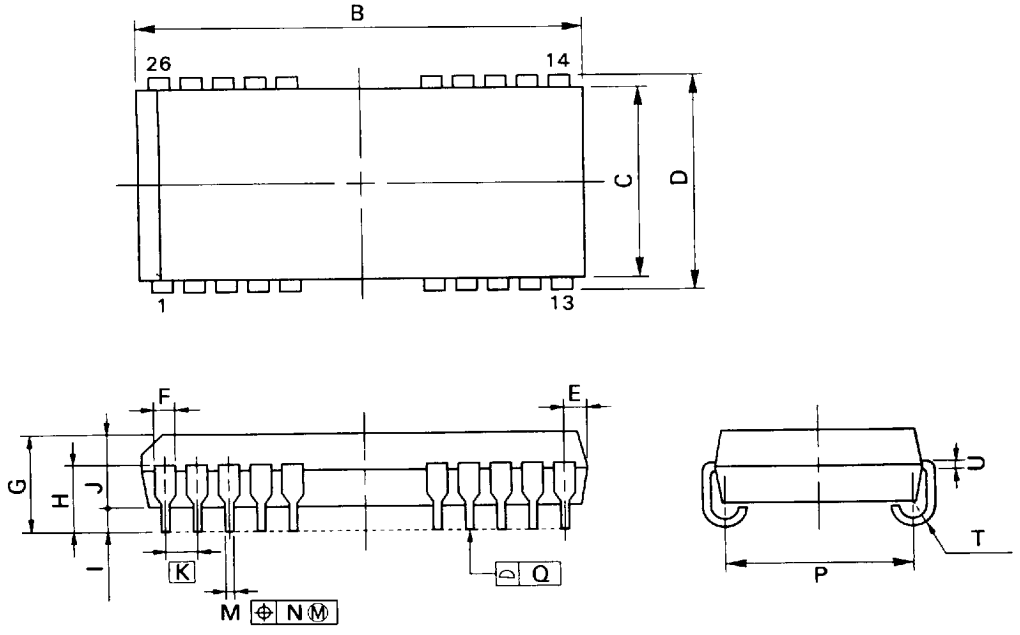
P26LA-50A-1

NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.4^{+0.2}_{-0.35}$	$0.685^{+0.008}_{-0.013}$
C	7.57	0.298
D	$8.47^{\pm 0.2}$	$0.333^{+0.009}_{-0.008}$
E	$1.08^{\pm 0.15}$	$0.043^{+0.006}_{-0.007}$
F	0.6	0.024
G	$3.5^{\pm 0.2}$	$0.138^{\pm 0.008}$
H	$2.4^{\pm 0.2}$	$0.094^{+0.009}_{-0.008}$
I	0.8 MIN	0.031 MIN.
J	2.6	0.102
K	1.27(T.P.)	0.050(T.P.)
M	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
N	0.12	0.005
P	$6.73^{\pm 0.20}$	$0.265^{\pm 0.008}$
Q	0.15	0.006
T	R 0.85	R 0.033
U	$0.20^{+0.10}_{-0.05}$	$0.008^{+0.004}_{-0.002}$

26PIN PLASTIC SOJ (350 mil)



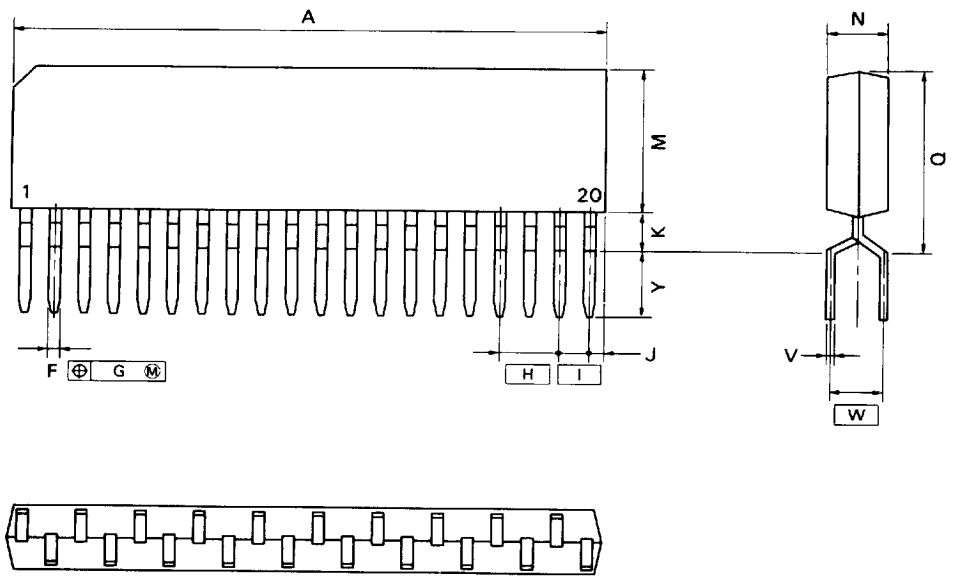
P26LB-350A

NOTE

Each lead centerline is located within 0.12 mm (0 005 inch) of its true position (T P) at maximum material condition.

ITEM	MILLIMETERS	INCHES
B	$17.4^{+0.2}_{-0.35}$	$0\ 685^{+0.008}_{-0.013}$
C	8 89	0 35
D	$9\ 78^{\pm 0.2}$	$0\ 385^{\pm 0.008}$
E	$1\ 08^{\pm 0.15}$	$0\ 043^{+0.006}_{-0.007}$
F	0 6	0.024
G	$3\ 6^{\pm 0.2}$	$0\ 142^{+0.008}_{-0.007}$
H	$2.45^{\pm 0.2}$	$0.096^{+0.009}_{-0.008}$
I	0 8 MIN	0 031 MIN
J	2 7	0 106
K	1.27 (T P)	0 050 (T P)
M	$0\ 40^{\pm 0.10}$	$0\ 016^{+0.004}_{-0.005}$
N	0 12	0 005
P	$8.06^{\pm 0.20}$	$0.317^{+0.008}_{-0.007}$
Q	0.15	0 006
T	R0 85	R0 033
U	$0\ 20^{+0.10}_{-0.05}$	$0\ 008^{+0.004}_{-0.002}$

20PIN PLASTIC ZIP (400 mil)



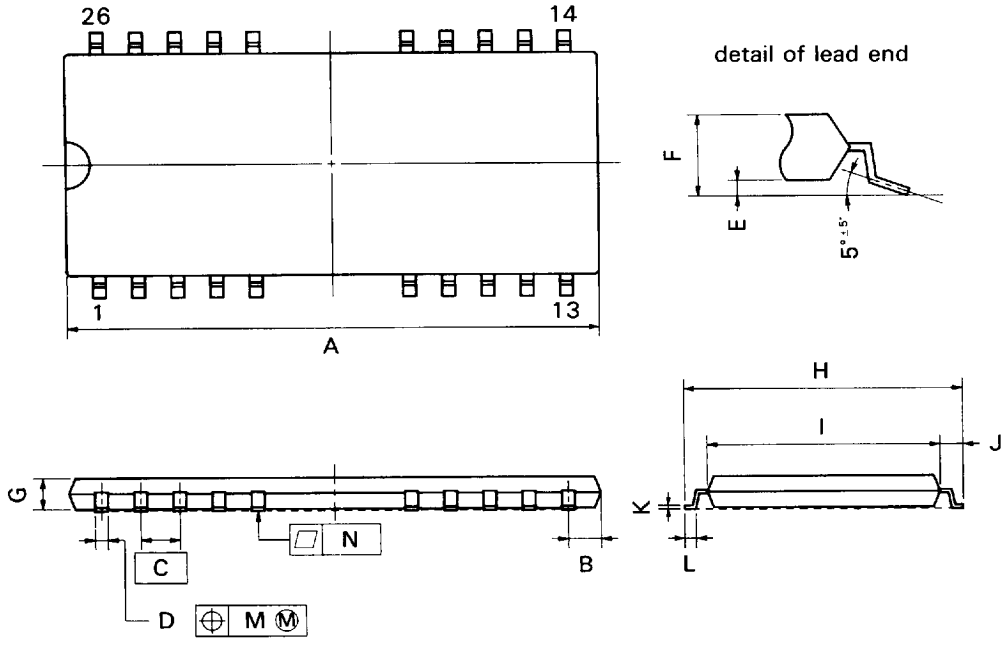
P20V-254-400A-1

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	26.67 MAX.	1.050 MAX.
F	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
G	ϕ0.25	ϕ0.010
H	2.54	0.100
I	1.27	0.050
J	1.27 MAX.	0.050 MAX.
K	1.0 MIN.	0.039 MIN.
M	8.9 MAX.	0.350 MAX.
N	$2.8^{\pm 0.2}$	$0.110^{+0.009}_{-0.008}$
Q	10.16 MAX.	0.400 MAX.
V	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
W	2.54	0.100
Y	$3.3^{\pm 0.5}$	$0.130^{\pm 0.02}$

26 PIN PLASTIC TSOP (300mil) ★



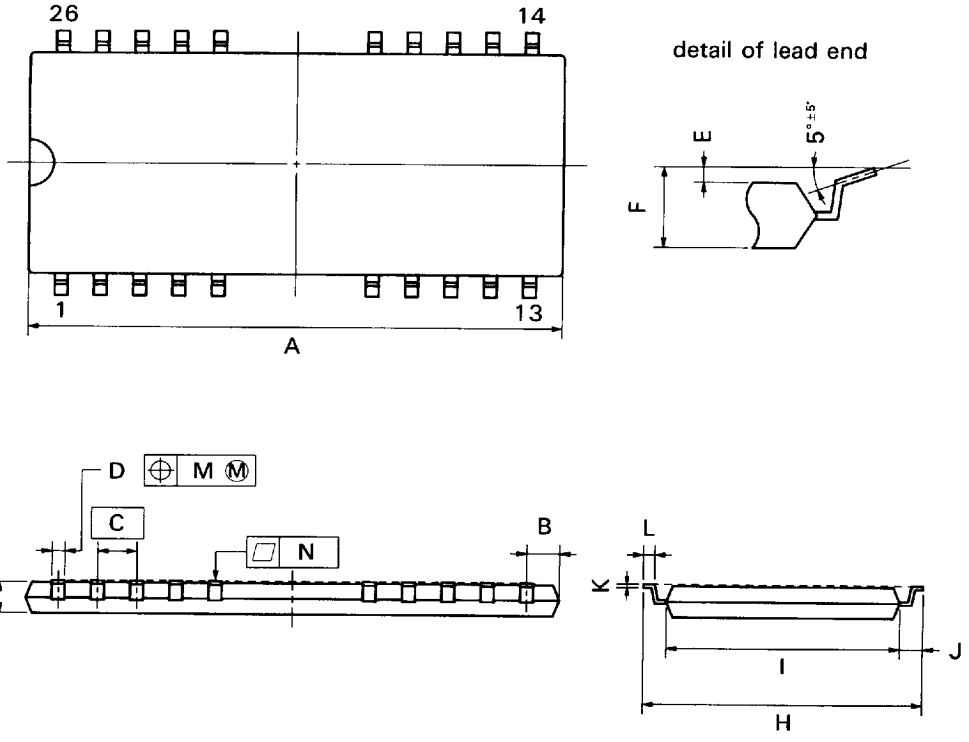
S26GS-50-9JD-1

NOTE

Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0.691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
E	$0.05^{\pm 0.05}$	$0.002^{\pm 0.002}$
F	1.13 MAX	0.045 MAX
G	1.0	0.039
H	$9.22^{\pm 0.2}$	$0.363^{\pm 0.008}$
I	$7.62^{\pm 0.1}$	$0.300^{\pm 0.004}$
J	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

26 PIN PLASTIC TSOP (300mil) ★



S26GS-50-9KD-1

NOTE
Each lead centerline is located within 0.21 mm (0.009 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.54 MAX.	0.691 MAX.
B	1.18 MAX.	0.047 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{\pm 0.10}$	$0.016^{+0.004}_{-0.005}$
E	$0.05^{\pm 0.05}$	$0.002^{\pm 0.002}$
F	1.13 MAX.	0.045 MAX.
G	1.0	0.039
H	$9.22^{\pm 0.2}$	$0.363^{\pm 0.008}$
I	$7.62^{\pm 0.1}$	$0.300^{\pm 0.004}$
J	$0.8^{\pm 0.2}$	$0.031^{+0.009}_{-0.008}$
K	$0.125^{+0.10}_{-0.05}$	$0.005^{+0.004}_{-0.002}$
L	$0.5^{\pm 0.1}$	$0.020^{+0.004}_{-0.005}$
M	0.21	0.009
N	0.10	0.004

RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering this product.

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

TYPES OF SURFACE MOUNT DEVICE

For more details, refer to our document "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

μPD424100LA ★

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 1, Exposure limit*: 7 days (10 hours pre-baking is required at 125 °C afterwards).	IR30-107-1
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 1, Exposure limit*: 7 days (10 hours pre-baking is required at 125 °C afterwards).	VP15-107-1
Partial heating method	Pin temperature: 300 °C or below, Flow time: 3 seconds or below. (for one side of the device).	Partial heating method

μPD424100LB ★

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 2, Exposure limit*: 7 days (20 hours pre-baking is required at 125 °C afterwards).	IR30-207-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2, Exposure limit*: 7 days (20 hours pre-baking is required at 125 °C afterwards).	VP15-207-2
Partial heating method	Pin temperature: 300 °C or below, Flow time: 3 seconds or below (for one side of the device).	Partial heating method

*: Exposure limit before soldering after dry-package is opened.

Storage conditions: 25 °C and relative humidity at 65 % or less.

μPD424100GS★

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C or below, Reflow time: 30 seconds or below (210 °C or higher), Number of reflow process: 2, Exposure limit*: 1 day (10 hours pre-baking is required at 125 °C afterwards).	IR30-101-2
VPS	Peak package's surface temperature: 215 °C or below, Reflow time: 40 seconds or below (200 °C or higher), Number of reflow process: 2, Exposure limit*: 3 days (10 hours pre-baking is required at 125 °C afterwards).	VP15-103-2
Partial heating method	Pin temperature: 300 °C or below, Flow time: 3 seconds or below. (for one side of the device).	Partial heating method

*: Exposure limit before soldering after dry-package is opened.
Storage conditions: 25 °C and relative humidity at 65 % or less.

Note: Do not apply more than a single process at once, except for "Partial heating method".

TYPE OF THROUGH HOLE MOUNT DEVICE

μPD424100V

Soldering process	Soldering conditions	Symbol
Wave soldering	Solder temperature: 260 °C or below, Flow time: 10 seconds or below	WS60-00